Teratronik
elektronische systeme gmbh

V4½-CPU
Technical Data

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Datum	Author	Änderungen
26.11.08	O. Wölfelschneider, Teratronik GmbH	Start

1. Features

V4½-CPU is a microcontroller based on the ARM9 architecture.

Features:

- Atmel AT91SAM9263 CPU (Arm 926EJ-S Core)
- 32 MiB SDRAM 16bit/100MHz
- 2 MiB battery backed static RAM
- 4 MiB serial Dataflash
- 64 MiB NAND Flash
- Socket for memory cards (up to 32GB)

Interfaces:

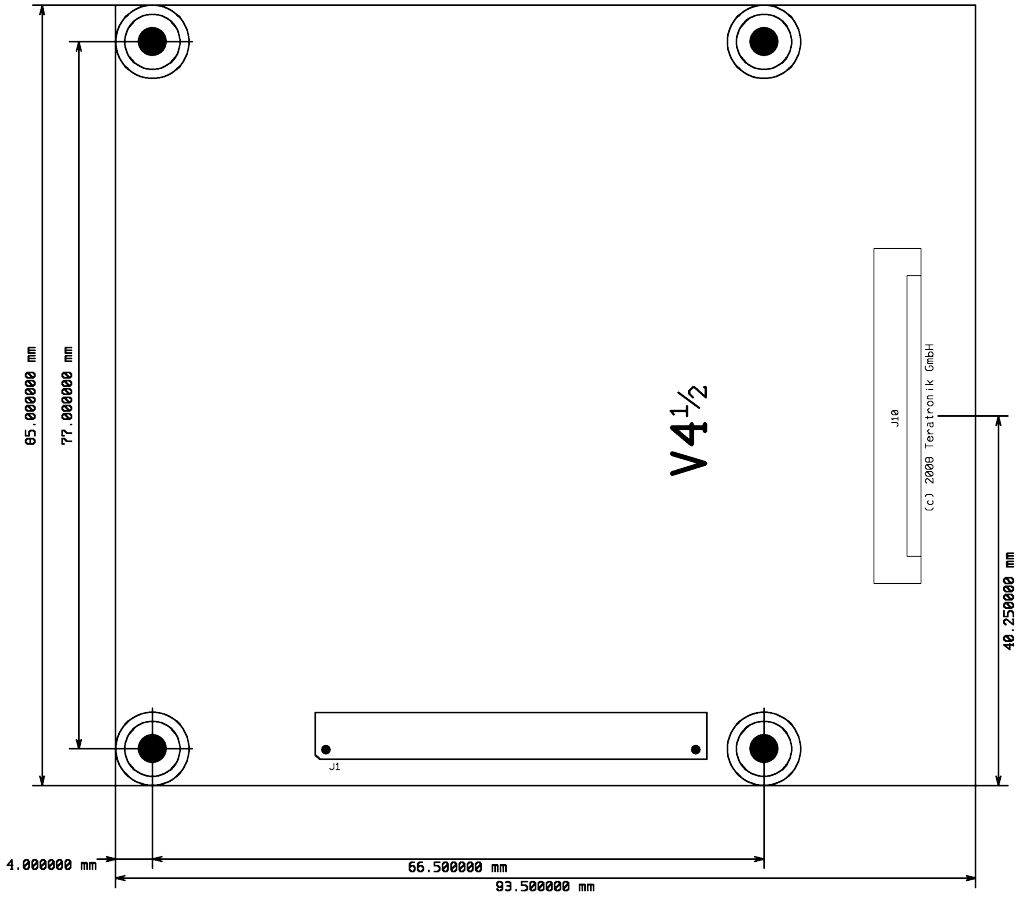
- TTL-RGB interface for TFT or OLED displays up to 800x480
- 4-wire touch screen interface
- 10/100 Ethernet Auto MDI-X
- 2 x USB Host ports
- 1 x USB Device port

Further interfaces are available on a 120pin board-to-board connector:
(All signals are 3,3V TTL, unless noted differently.)

- 1 x RS232 serial port (RS232 levels, DBGU - Serial Debug Port)
- 5 x serial port TTL
- AC97 audio codec
  - Microphone input (Mono, with 3V power for electret mic)
  - 1W amplifier (Mono, 8Ω)
  - Stereo line-out
  - Stereo line-in
  - SPDIF-out (undriven TTL)
- TWI-port (I²C compatible)
- SPI-port with four chip-selects
- TTL I/O ports
- Power management interface (wakeup, shutdown)

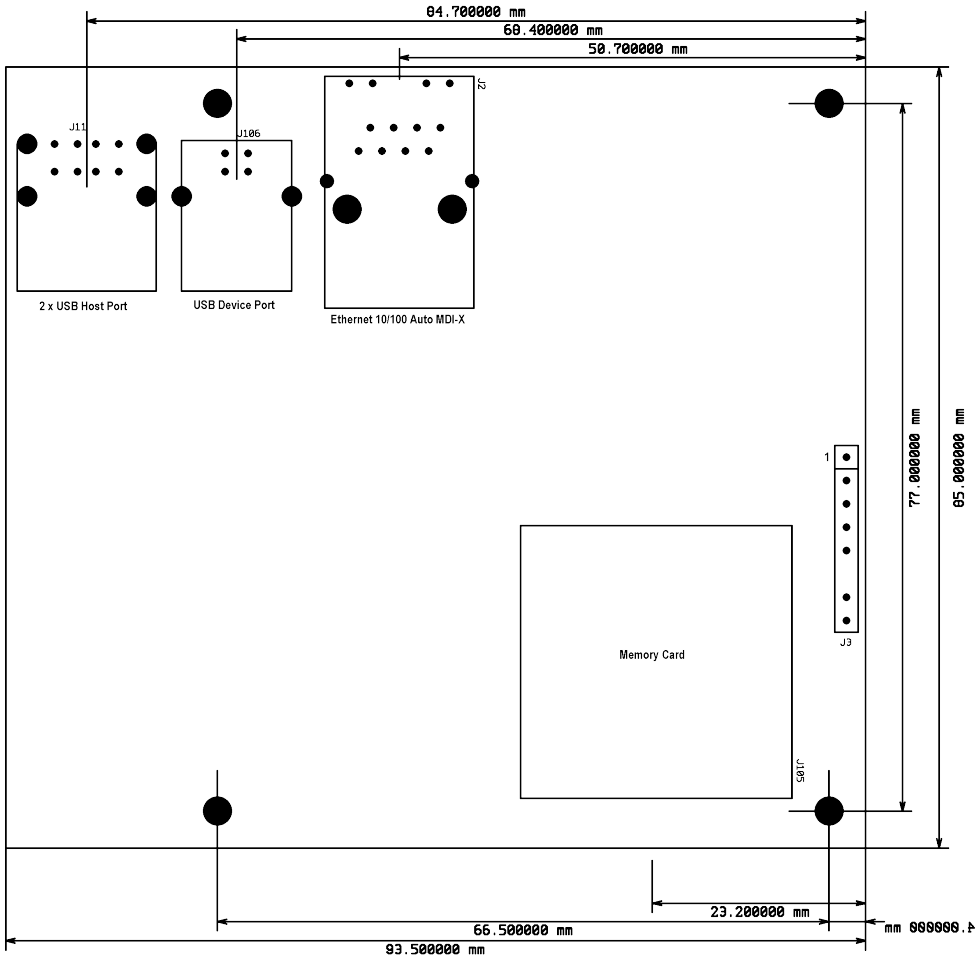
2. Views

Top view:



J1 - 120pin board to board connector
J10 - 60pin display connector (TTL-RGB)

Bottom view:

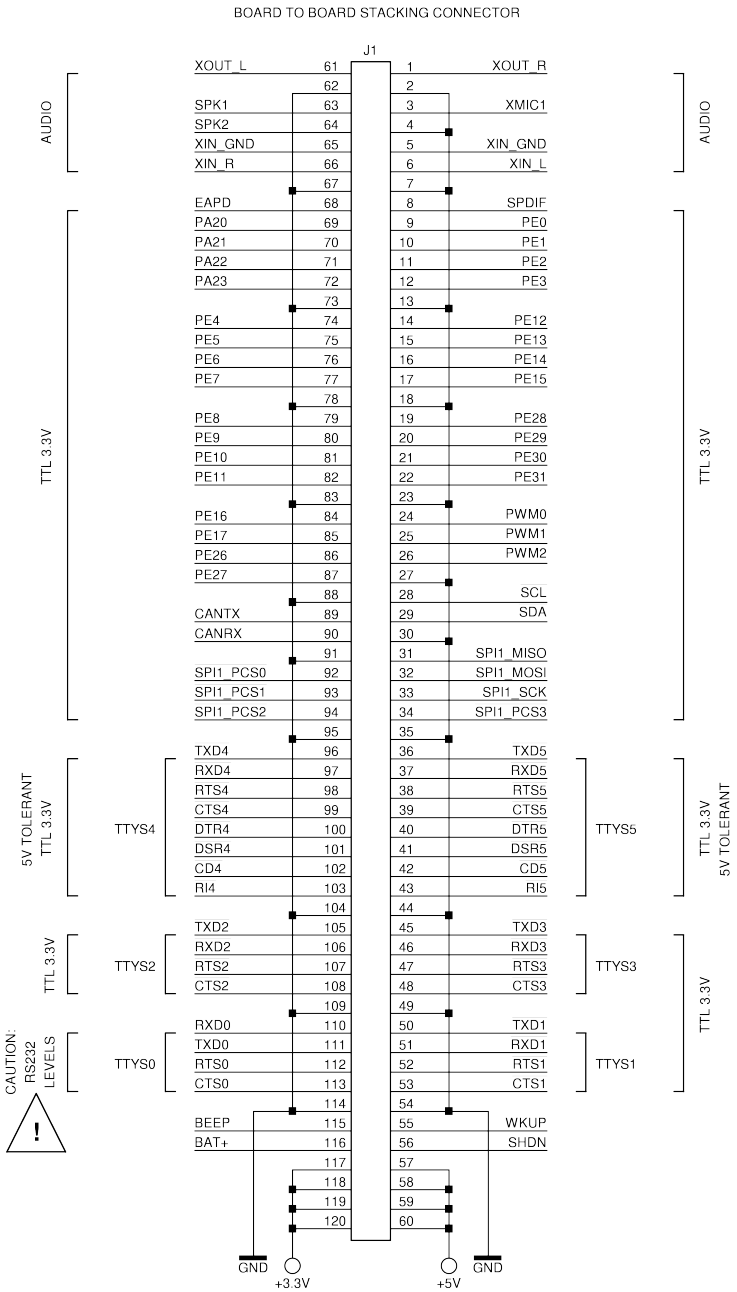


J2 - 10/10/100 ethernet auto MDI-X
J3 - Download helper
J11 - 2 x USB host ports
J106 - USB device port

3. Connector pinouts

3.1 J1 - board-to-board connector

This connector accepts adapter boards that supply power and provide further interface connections.



The mating connector needed is Hirose FX8C-120S-SV5.

Power supply

This board runs on single +5V supply. A built in regulator converts to 3.3V and provides it to J1.

Never connect an external voltage to the 3.3V pins at J1.

Data backup

The board includes a Goldcap capacitor to provide backup power for the built in clock and the static RAM. This capacitor is good for a few hours backup.

It is recommended to connect a 3V lithium battery to J1, pin 116 to provide longer backup.

Battery power is only consumed if the main power supply is off.

Power management

Pins 55 (WKUP) and 45 (SHDN) provide access to the CPU's built in power management. These pins are supplied by an internal 1.2V voltage from the battery backup supply. Do not connect any TTL signals to these pins. Consult the CPU manual before use.

Buzzer

Peripheral	*Device*	*Channel*	*Pinout*			*Comment*
Timer0	AT91SAM9263	TIOA0	BEEP	PE18	115	3.3V TTL

Can be used to drive a piezo buzzer using a driver transistor. Idle state is L.

Serial ports

Port	*Device*	*Channel*	*Pinout*			*Comment*
ttyS0	AT91SAM9263	DBGU	RxD	PC30	110	**RS232 signal levels**
			TxD	PC31	111	
			RTS	PB28	112	
			CTS	PB31	113	
ttyS1	AT91SAM9263	USART0	RxD	PA27	51	3.3V TTL
			TxD	PA26	50	
			RTS	PA28	52	
			CTS	PA29	53	
ttyS2	AT91SAM9263	USART1	RxD	PD1	106	3.3V TTL
			TxD	PD0	105	
			RTS	PD7	107	
			CTS	PD8	108	
ttyS3	AT91SAM9263	USART2	RxD	PD3	46	3.3V TTL
			TxD	PD2	45	
			RTS	PD5	47	
			CTS	PD6	48	

Port	*Device*	*Channel*	*Pinout*			*Comment*
ttyS4	XR16L2750	A	CS	EBI1_NCS0		Goes to CPU
			INT	PA3		
			RxD		97	3.3V TTL 5V tolerant
			TxD		96	
			RTS		98	
			CTS		99	
			DTR		100	
			DSR		101	
			CD		102	
			RI		103	
ttyS5	XR16L2750	B	CS	EBI1_NCS1		Goes to CPU
			INT	PA4		
			RxD		37	3.3V TTL 5V tolerant
			TxD		36	
			RTS		38	
			CTS		39	
			DTR		40	
			DSR		41	
			CD		42	
			RI		43	

SPI Port

Peripheral	*Device*	*Channel*	*Pinout*			*Comment*
SPI	AT91SAM9263	SPI1	MISO	PB12	31	3.3V TTL
			MOSI	PB13	32	
			SCK	PB14	33	
			NCS0	PB15	92	
			NCS1	PB16	93	
			NCS2	PB17	94	
			NCS3	PB18	34	

CAN Interface

Peripheral	*Device*	*Channel*	*Pinout*			*Comment*
CAN	AT91SAM9263	CAN	CANTX	PA13	89	3.3V TTL
			CANRX	PA14	90	

TWI Interface

Peripheral	*Device*	*Channel*	*Pinout*			*Comment*
TWI	AT91SAM9263	TWI	SCL	PB5	28	3.3V TTL
			SDA	PB4	29	

PWM outputs

Peripheral	*Device*	*Channel*	*Pinout*			*Comment*
PWM	AT91SAM9263	PWM	PWM0	PB7	24	3.3V TTL
			PWM1	PB8	25	
			PWM2	PB27	26	

TTL IO

Peripheral	*Device*	*Channel*	*Pinout*		*Comment*
GPIO	AT91SAM9263	PORTE	PE0	9	3.3V TTL
			PE1	10	
			PE2	11	
			PE3	12	
			PE4	74	
			PE5	75	
			PE6	76	
			PE7	77	
			PE8	79	
			PE9	80	
			PE10	81	
			PE11	82	
			PE12	14	
			PE13	15	
			PE14	16	
			PE15	17	
			PE16	84	
			PE17	85	
			PE26	86	
			PE27	87	
			PE28	19	
			PE29	20	
			PE30	21	
			PE31	22	

Peripheral	*Device*	*Channel*	*Pinout*		*Comment*
GPIO	AT91SAM9263	PORTA	PA20	69	3.3V TTL
			PA21	70	
			PA22	71	
			PA23	72	

AC97 Audio

Peripheral	*Device*	*Channel*	*Pinout*		*Comment*
AC97	WM9705	CD input	XIN_L	6	Connect XIN_GND to GND at the signal source.
			XIN_R	66	
			XIN_GND	5 & 65	
		Mono output	SPK1	63	Amplified 1W 8Ω
			SPK2	64	
		MIC1	XMIC1	3	With 3V power for electret microphone.
		Line out	XOUT_L	61	
			XOUT_R	1	
		Amp power	EAPD	68	H = Amplifier on

To enable AC97 it is necessary to drive PB23 (ISOLATE) low by software.

The EAPD signal is connected inverted regarding the AC97 standard to avoid clicking noises at powerup.

The touch screen controller included in the WM9705 is routed to the display connector. The touch screen interrupt is connected to PB21 (SND_PEN_INT).

3.2 J2 - Ethernet 10/100

This is a standard RJ45 ethernet jack.

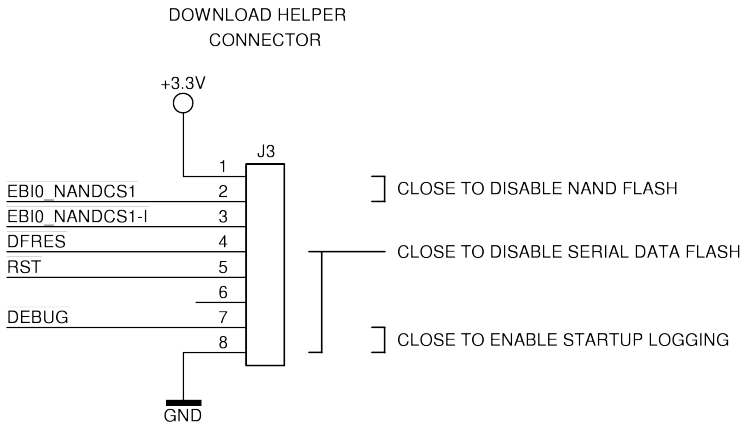
This port supports auto MDI-X. You can connect it with a single other device without the need for a switch or a special cable.

The built in ethernet controller of the AT91SAM9263 cannot be used as it is blocked by some signals running to the RGB-TTL display connector.

Therefore, this design uses a Davicom DM9000A ethernet MAC+PHY.

The DM9000A is selected by EBI0_NCS0 and connected with 16bit width. It raises interrupts on PA15.

3.3 J3 - Download helper connector



Used to temporary disable on board flash memories. Useful for 'reviving' a dead board that was bricked by loading it with a malfunctioning software.

To disable the NAND flash, connect pins 1+2.

To disable the serial dataflash, connect pins 4+8.

Pin 7 selects the behaviour of the serial debug port (DBGU, ttyS0).

No jumper:

DBGU is a normal serial port.

Portpin PA17 ist pulled **high**. (So software can detect this jumper.)

Serial port DBGU cannot send data until PB23 (ISOLATE) is driven low by software.

Jumper between 7+8:

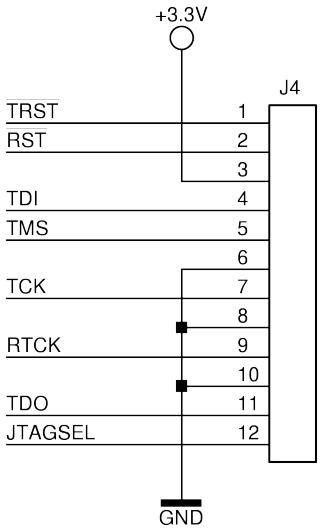
DBGU is used as the kernel log console.

Portpin PA17 ist pulled **low**. (So software can detect this jumper.)

Serial port DBGU is always enabled to send.

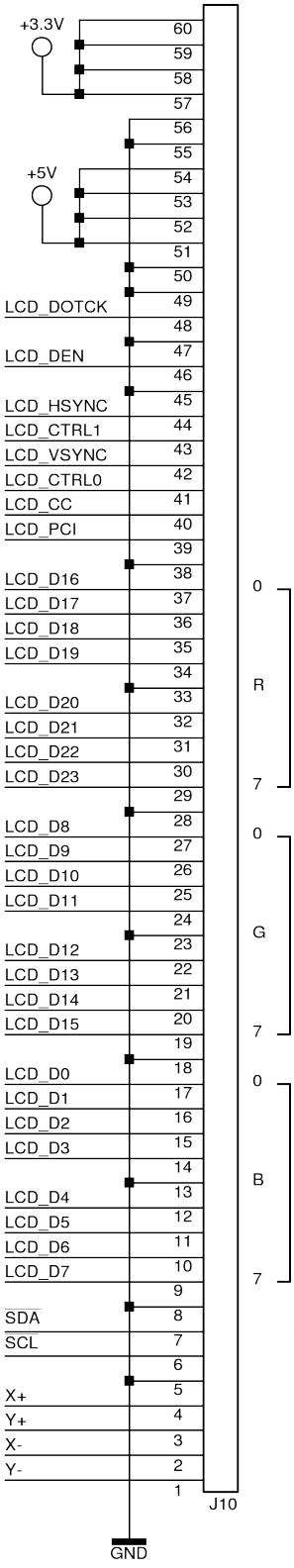
3.4 J4 - JTAG connector

12pin FFC Connector 0.5mm Pitch.



Only mounted on development boards. Adapter to standard 20pin JTAG header is available on request.

3.5 J10 - RGB-TTL display connector



This connector provides a full 24-bit RGB-TTL interface.

Provides +5V and +3.3V for powering the display.

Also provides access to the SDA/SCL TWI-interface and some general purpose ports.

Pinout			***Description***
DOTCK	PC2	48	Pixel clock
DEN	PC3	46	Data-enable
HSYNC	PC1	44	Horizontal-sync
CTRL1	PE24	43	General purpose
VSYNC	PC0	42	Vertical-sync
CTRL0	PE21	41	General purpose
CC	PB9	40	'ContrastControl' PWM-output for brightness.
PCI	PB29	39	'PowerControlInput' General purpose
D16 - D23	PC20 - PC27		Red
D8 - D15	PC12 - PC19		Green
D0 - D7	PC4 - PC11		Blue
SDA	PB4	7	TWI interface, 3.3V TTL
SCL	PB5	6	
X+	to WM9705 Codec	4	4-wire touch screen
Y+		3	
X-		2	
Y-		1	

Note: Connections for red & blue are swapped regarding the AT91SAM9263 datasheet. This enables software to use the more common RGB pixel format instead of BGR.

3.6 J11 - USB host port

USB-A double jack using standard pinout.

Hardware includes built-in overload protection that can switch off each port separately.

Overload protection connects to the CPU using these signals:

USB-Port	*Signal*			*Description*
Port A (top)	USB_ENA	PB19	from CPU (Out)	H = Turn power supply on
	USB_FLGA	PB22	to CPU (In)	H = Port overload, powered off
Port B (bottom, closer to PCB)	USB_ENB	PB20	from CPU (Out)	H = Turn power supply on
	USB_FLGB	PB11	to CPU (In)	H = Port overload, powered off

3.7 J105 - Socket for memory cards.

This socket accepts common memory cards. Compatible with MMC, SD-Card and SDHC.

Signal		*Beschreibung*
CK	PA6	Clock, up to 20MHz.
CDA	PA7	Command/Data
DA0	PA8	Data bits
DA1	PA9	
DA2	PA10	
DA3	PA11	
WP	PB26	H = Card write protected
CD	PB30	L = Card is inserted

3.8 J106 - USB device port

USB-B Jack with standard pinout.

Signal USBCNX provides H level to PB25 if there is a connection present.

4. Internal signals

4.1 LEDs

There are three LEDs at the left board edge:

Peripheral	*Device*	*Channel*			*Description*
GPIO	AT91SAM9263	LED1	PC28	Red	L = LED on
		LED2	PC29	Green	
		LED3	PA19	Yellow	

4.2 Dataflash

Board contains an AT45DB321D serial dataflash. The chip is connected to SPI0 and can be booted from.

Peripheral	*Device*	*Channel*	*Pinout*		*Description*
SPI	AT91SAM9263	SPI0	MISO	PA0	3.3V TTL
			MOSI	PA1	
			SCK	PA2	
			NCS0	PA5	
GPIO	AT91SAM9263	PORTB	DFBUSY	PB6	L = Busy

4.3 NAND flash

The NAND-flash chip is connected to the NAND-flash-controller at bus EBI0.

Board can boot from this chip.

By default, a Samsung K9F1G08U0B-PIB with 64MB is mounted.

Board is prepared to take multi-chip-modules with up to four chips in a package. For that purpose, there are four chip selects and four ready/busy lines.

Device	*Signal*			*Description*
Standard	NANDCS1	PD15	from CPU (Out)	L = ChipSelect
	RDYBSY1	PD14	to CPU (In)	L = Busy
2nd chip	NANDCS2	PD9		Not used in standard version.
	RDYBSY2	PD10		
3rd chip	NANDCS3	PD12		
	RDYBSY3	PD13		
4th chip	NANDCS4	PA18		
	RDYBSY4	PA16		

4.4 Miscellaneous

PB23 (ISOLATE)

Isolates parts of the hardware from the CPU until the firmware has initialized.

After RESET, this signal is H, which means:

- PB3 is disconnected from AC97 and pulled H.
  Makes sure the on-chip boot program can run.

- Transmitting direction of DBGU (ttyS0) is disabled.
  This suppresses the text 'RomBoot' that is sent by the on-chip boot program.

The firmware must program PB23 to L.

PA17 (DEBUG)

Inputs L if pins 7+8 of J3 are connected with a jumper.